Instruction Manual

Tektronix

TCS101
SPI-3 and SPI-4.2 Bus Software Support

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www.tektronix.com

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Table of Contents

Getting Started

Operating Basics

Reference

Specifications

Index

List of Figures

List of Tables

Preface

This instruction manual contains specific information about the TCS101 software product for the SPI-3 and SPI-4.2 buses and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer for which the TCS101 product was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating bus support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of bus support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of logic analyzer online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into packets and control information.
- The phrase “basic operations” refers to the logic analyzer online help, or the user manual that covers the basic operations of the bus support.
- The phrase “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

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*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TCS101 product and information on connecting your logic analyzer to your target system.

Support Package Description

The TCS101 product acquires, decodes and displays the SPI-3 and SPI-4.2 bus cycles. The support package allows you to acquire bus cycles with minimal impact on the environment of the system.

The TCS101 product contains four acquisition support packages that have their own setup software and disassemblers. A description of each support package is listed here.

- SPI3_TX, for the SPI-3 Transmit Interface
- SPI3_RX, for the SPI-3 Receive Interface
- SPI4, for the SPI-4.2 Transmit and Receive interfaces with LVDS FIFO Status signals
- SPI4_LVTTL, for the SPI-4.2 Transmit and Receive interfaces with LVTTL FIFO Status signals

Disassembly Support

The disassembler decodes transmit and receive bus information of SPI-3 and SPI-4.2 buses.

The SPI3_TX and SPI3_RX support packages acquire and decode bus behavior at each clock cycle or at active clock cycles (see page 2–3). For SPI4 and SPI4_LVTTL support packages, the bus behavior is acquired at all clock cycles and decoded.

The disassembler decodes data in the following stages.

- Packet related information — start of packet, end of packet, payload (packet data), physical port address, packet continuation and packet error (DIP-4)
- Control information, Training, and Idle information
- FIFO Status decoding in SPI4 and SPI4_LVTTL with DIP-2

The payloads are indexed with byte counts corresponding to a port address, so that you can know how many bytes of data have been transmitted by or received at a port.

The ASCII characters corresponding to the payloads can be viewed by choosing "Decode Payload as ASCII" option (on pages 2–8 and 2–9) in the bus specific fields.

The SPI3_TX and SPI3_RX support packages display the calculated parity bit for each valid 8-bit or 32-bit data on the data bus.

After acquisition, the TCS101 product supports filtering based on the physical port address (see pages 2–7 and 2–8).

To use this support package efficiently refer to the following documents:

- *System Packet Interface Level 3 (SPI-3): OC-48 System Interface for Physical and Link Layer Devices {Optical Internetwork Forum, June 2000, OIF-SPI3-01.0}*
- *POS-PHY Level 3, Saturn Compatible Packet Over SONET Interface Specification for Physical and Link Layer Devices {PMC-Sierra Inc., Issue 4: June 2000, PMC-1980495}*
- *System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer Devices {Optical Internetwork Forum, January 2001, OIF-SPI4-02.0}*
- *POS-PHY Level 4, A Saturn Packet and Cell Interface Specification for OC192 SONET/SDH and 10 Gigabit Ethernet {PMC-Sierra Inc., Issue 6: February 2001, PMC-1991635}*

Triggering Support

The SPI3_TX and SPI3_RX support packages provide an EasyTrigger library to trigger on Port Address, control signals like Start-of-Packet and End-of-Packet, Erroneous Packet, and 8-bit or 32-bit Packet Data. The SPI4 and SPI4_LVTTL support packages provide an EasyTrigger library to trigger on control words and packet data.

Logic Analyzer Software Compatibility

The label on the bus support CD-ROM states which version of logic analyzer software this support package is compatible with.

Logic Analyzer Configuration

The TCS101 product allows a choice of required minimum module configurations.

Module Requirements

Table 1–1 shows the module requirements for the TCS101 product.

Table 1-1: Module requirements for the TCS101 product

Bus	Module requirements	Remarks
SPI-3	One module of : TLA7xx logic analyzer module at 200 MHz — 68 channel and above TLA6xx series logic analyzer at 200 MHz — 68 channel and above TLA7Axx series logic analyzer at 120 MHz — 68 channel and above	Minimum of one 68-channel logic analyzer module each for Transmit and Receive interfaces*
SPI-4.2	One module of : TLA7Axx logic analyzer module at 450 MHz — 102 channel and above	Minimum of one 102 channel TLA7Axx module Two 102 channel modules are required for a Transmit and Receive pair

*** You cannot use a single 102 or 136 channel module for loading the TX and RX interfaces together as the SPI3_TX and SPI3_RX support packages assume independent clocks.**

Probe Requirements

Table 1-2 shows the probe requirements for the TCS101 product.

Table 1-2: Probe requirements for the TCS101 product

Bus	Probes for TX or RX interface	Description
SPI-3	Two P6434 or P6860 probes	-
SPI-4.2	Two or three P6880 probes	Two P6880 probes are required for data One optional probe for FIFO status — either a P6880 probe for LVDS or LVTTL Status or a P6860 probe for LVTTL Status

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section on page 4-1 in this manual as they pertain to your target system, as well as the following descriptions of TCS101 product requirements and restrictions.

Hardware Reset

If a hardware reset occurs in your target system during an acquisition, the application disassembler might acquire an invalid sample.

Clock Rate

The TCS101 product can acquire data from the SPI-3 bus operating at 104 MHz. The TCS101 product can acquire data from the SPI-4.2 bus operating at 350 MHz[1].

FIFO Status Decoding

In the SPI4 and SPI4_LVTTL support packages, the FIFO Status decoding is displayed correctly only under the following conditions.

- Port Address Filter option is set to "No" in the disassembly properties tab
- Show option is set to "All" in the disassembly properties tab
- Filter Idles option is set to "Is False" for the EasyTrigger that was used to acquire the data

Setup/Hold Time Requirements

Table 1–3 lists the setup/hold time requirements for the different support packages. For correct acquisition, the target system must provide a data valid window meeting these requirements.

Table 1–3: Setup/Hold time requirements for the TCS101 product

Support package name	Logic analyzer/ module	Setup time	Hold time
SPI3_TX, SPI3_RX	TLA6xx/7xx	2.5 ns	0 ns
SPI3_TX, SPI3_RX	TLA7Axx	750 ps	0 ps
SPI4, SPI4_LVTTL	TLA7Axx	750 ps	0 ps

For SPI-4.2 supports, some of the target systems may require an adjustment in the Setup/Hold time settings of logic analyzer to match their data valid window.

Nonintrusive Acquisition

The TCS101 product acquires bus cycles nonintrusively from the target system. That is, the TCS101 product does not intercept, modify, or present signals back to the target system.

Limitations of the Support

The TCS101 product does not decode the embedded protocols.

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest bus supported.**

Connecting the Logic Analyzer to a Target System

You can use the channel probes and clock probes to make the connections between the logic analyzer and your target system.

To connect the probes to the SPI-3 and SPI-4.2 bus signals described in the TCS101 product channel assignment to the target system, follow the steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the target systems, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the target system.

2. Place the target system on a horizontal, static-free surface.
3. Use Tables 3–69 through 3–76 starting on page 3–39 to connect the channel probes to the SPI-3 and SPI-4.2 signals in the target system.

Labeling P6880 and P6860 Probes

The TCS101 product relies on the channel mapping and labeling scheme for the P6880 and P6860 Probes. Apply labels, using the instructions described in the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual.

Operating Basics

Setting Up the Support

This section provides information on how to set up the software support and covers the following topics:

- Installing the support software
- Support package setups
- Clocking options

The information in this section pertains to the specific operations and functions of the TCS101 product on a Tektronix logic analyzer for which the support can be used.

Before you acquire and display disassembled data, you need to load the support package and specify the setups for clocking and triggering as described in the logic analyzer online help under “Microprocessor support”. The support package provides default values for each of these setups, but you can change the setups as needed.

Installing the Support Software

***NOTE**. Before you install any software, it is recommended you verify that the bus support software is compatible with the logic analyzer software.*

To install the TCS101 product on your Tektronix logic analyzer, follow these steps:

1. Insert the CD-ROM in the CD drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the CD-ROM. A copy of the instruction manual is available on the CD-ROM.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

The TCS101 product installs four different support packages.

Support Package Setups

The TCS101 product installs four acquisition support packages that have their own setup software and disassemblers. A description of each support package is listed here.

- SPI3_TX: Use this support package to acquire SPI-3 transmit bus traffic. The support package decodes the acquired data and labels the bus cycles in a packet style display. The package supports 8-bit and 32-bit buses.
- SPI3_RX: Use this support package to acquire SPI-3 receive bus traffic. The support package decodes the acquired data and labels the bus cycles in a packet style display. The package supports 8-bit and 32-bit buses.
- SPI4: Use this support package to acquire SPI-4.2 bus traffic. The support package acquires the FIFO Status bus using LVDS signaling. It can be used with the transmit or receive interfaces. It decodes the acquired data and labels the bus cycles in a packet style display.
- SPI4_LVTTL: Use this support package to acquire SPI-4.2 bus traffic. The support package acquires the FIFO Status bus using LVTTL signaling. It can be used with the transmit or receive interfaces. It decodes the acquired data and labels the bus cycles in a packet style display.

The TCS101 product adds these four selections to the “Load Support Package” dialog box, under the File pulldown menu.

Clocking Options

A special custom clocking program is loaded into the module every time you load one of the SPI3_TX, SPI3_RX, SPI4, and SPI4_LVTTL support packages from the TCS101 product. Each support package offers different clocking options. You may use the default clocking option or choose an alternate by clicking the “More...” button in the logic analyzer setup window.

SPI3_TX and SPI3_RX

The software provides two custom clocking options for the SPI3_TX and SPI3_RX support packages.

Cycles. The Cycles option provides the following choices:

- “All” is for storing data on every clock cycle (default).
- “Active Only” is for storing data only when the data bus is valid.

Physical Port. The Physical Port option provides the following choices:

- "Single-No InBand Addr" is for a single physical port without TSX or RSX signals (default).
- "Single With InBand Addr" is for a single physical port with TSX or RSX signals.
- "Multiple" is for multiple physical port interfaces. This option uses TSX or RSX and PTPA signals, including byte level and packet level transfer modes.

SPI4 and SPI4_LVTTL

The software provides one custom clocking option for SPI4 and SPI4_LVTTL support packages:

All Cycles. "All Cycles" is for storing data on every clock cycle.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Changing the way data is displayed
- Labels for bus cycles
- Viewing disassembled data in various display formats

Acquiring Data

The TCS101 product for the SPI-3 and SPI-4.2 bus installs four different supports: SPI3_TX, SPI3_RX, SPI4, and SPI4_LVTTL.

Once you load the support package, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help.

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to fit your needs. You can make common and optional display selections in the Disassembly property page.

You can make selections unique to the support package from the TCS101 product to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

Tables 2–1 through 2–2 show the disassembly display options for the SPI-3 and SPI-4.2 support packages.

Table 2–1: Logic analyzer disassembly display options for SPI3_TX and SPI3_RX support packages

Description	Option
Show	All (default) Packet
Highlight	All (default)
Disassemble Across Gaps	Yes No (default)

Table 2–2: Logic analyzer disassembly display options for SPI4 and SPI4_LVTTL support packages

Description	Option
Show	All (default) Packet & Control Packet Only
Highlight	All (default)
Disassemble Across Gaps	Yes No (default)

Bus Specific Fields

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways.

Table 2–3 lists the bus specific fields for SPI3_TX and SPI3_RX support packages.

Table 2–3: Bus specific fields for SPI3_TX and SPI3_RX support packages

Field	Definition
Port Address Filter	Choose whether to filter the acquired data sent to or received from a port
Port Address	Enter the port address in hexadecimal
Physical Port Configuration	Select the physical port configuration
Cycles	Select cycles to decode data*
Data Bus Width	Select the data bus width in bits

Table 2-3: Bus specific fields for SPI3_TX and SPI3_RX support packages (Cont.)

Field	Definition
Decode Payload as ASCII	Choose to decode payload information in ASCII

* **Applicable only for the SPI3_RX support package**

Port Address Filter. Select the Port Address Filter as one of the following:

No (default)
Yes

Set this option to Yes if you want to filter the acquired data sent to or received from a selected physical port.

Port Address. Select the Port Address if you want to filter the acquired data sent to or received from the port. The default value is 00.

You can enter a maximum value of FF in hexadecimal for the Port Address.

Physical Port Configuration. Select the Physical Port Configuration as one of the following:

Single - No InBand Addr (default)
Single with InBand Addr
Multiple

For correct disassembly, set the Physical Port Configuration to match with the custom clocking option selected during acquisition.

Cycles. Select the Cycles as one of the following:

All (default)
Active Only

Set this option to All to decode data on every clock cycle, and Active Only to decode data only when the data bus is valid.

For correct disassembly, set the Cycles to match with the custom clocking option selected during acquisition.

***NOTE**. The bus specific field Cycles is used only in the SPI3_RX support package.*

Data Bus Width. Select the Data Bus Width as one of the following:

8 bits (default)
32 bits

Decode Payload as ASCII. Select Decode Payload as ASCII as one of the following options:

Yes (default)
No

Set this option to Yes if you want to see the payload information in ASCII.

Table 2–4 lists the bus specific fields for SPI4 and SPI4_LVTTL support packages.

Table 2–4: Bus specific fields for SPI4 and SPI4_LVTTL support packages

Field	Definition
Port Address Filter	Choose whether to filter the acquired data sent to or received from a port
Port Address	Enter the port address in hexadecimal
Decode Payload as ASCII	Choose to decode payload information in ASCII
Calendar_LEN	Enter the length of the calendar sequence
Calendar_M	Enter the number of times a calendar sequence is repeated between insertions of framing pattern

Port Address Filter. Select the Port Address Filter as one of the following:

No (default)
Yes

Set this option to Yes if you want to filter the acquired data sent to or received from a selected physical port.

Port Address. Select the Port Address if you want to filter the acquired data sent to or received from the port. The default value is 00.

You can enter a maximum value of FF in hexadecimal for the Port Address.

Decode Payload as ASCII. Select Decode Payload as ASCII as one of the following options:

Yes (default)
No

Set this option to Yes if you want to see the payload information in ASCII.

Calendar_LEN. Enter the Calendar_LEN value. You can enter a maximum value of 256 in decimal format. The default value is 1.

Calendar_M. Enter the Calendar_M value. You can enter a maximum value of 256 in decimal format. The default value is 1.

Labels for Bus Cycles

The TCS101 product decodes and displays the bus behavior in the Packet/Cell Details (Mnemonic) column in SPI3_TX, SPI3_RX, SPI4 and SPI4_LVTTL support packages.

Table 2–5 lists the labels displayed in the Packet/Cell Details column in the listing window for the SPI3_TX and SPI3_RX support packages.

Table 2–5: Labels in Packet/Cell Details column for SPI3_TX and SPI3_RX support packages

Label	Description
INVALID DATA	Invalid data on the SPI-3 data bus
PORT ADDRESS : (*Port Address in hex*)	Physical port address
UNRECOGNIZED DATA	Control group value of an acquired sample does not match the control symbol table
SHORT LENGTH PACKET	Packet data at which EOP and SOP signals asserted at same clock edge
ERRONEOUS PACKET	Packet data at which the TERR or RERR signals are asserted
START OF PACKET	Packet start
END OF PACKET	Packet end
PAYLOAD : (*Index in decimal*) : (*Hex value of the payload*)	Packet data

Table 2–6 lists the labels displayed in the Packet/Cell Details column in the listing window for the SPI4 and SPI4_LVTTL support packages.

Table 2–6: Labels in Packet/Cell Details column for SPI4 and SPI4_LVTTL support packages

Label	Description
START OF PACKET (ADDR: *port address in hex*)	Packet start
END OF PACKET (ADDR: *port address in hex*)	Packet end
PACKET CONTINUES (ADDR: *port address in hex*)	Packet continuation
VALID CONTROL WORD	Valid control word
IDLE CONTROL WORD	Idle control word
TRAINING	Training word
Type : (*Control word type*)	Control word "Type"
Port Address : (*Port address in hex*)	Physical port address
DIP-4 : (*DIP-Value*)	Diagonal Interleaved Parity Calculation (4-bit)
PAYLOAD (*Index in decimal*) : (*Hex value of the Payload*)	Payload details

Table 2–7 lists the labels displayed in the FIFO Status column in the listing window for the SPI4 and SPI4_LVTTL support packages.

Table 2–7: Labels in FIFO Status column for SPI4 and SPI4_LVTTL support packages

Label	Description
STARVING	Transfer up to Max Burst 1
HUNGRY	Transfer up to Max Burst 2
SATISFIED	FIFO is almost full
SYNC	Calendar follows
DISABLED	Disabled
TRAINING	-
DISABLED/TRAINING	Unidentified FIFO Status
DIP-2	Diagonal Interleaved Parity Calculation (2-bit)
CAL[*Calendar_LEN index in decimal*]:	Calendar length prefixed to STARVING, HUNGRY or SATISFIED

Viewing Disassembled Data

You can view disassembled data for the SPI3_TX and SPI3_RX support packages in two display formats:

All
Packet

You can view disassembled data for the SPI4 and SPI4_LVTTL support packages in three display formats:

All
Packet & Control
Packet Only

Always select the All display format for viewing correctly disassembled FIFO Status data.

The information on basic operations describes how to select the disassembly display formats.

***NOTE**. You must set the selections in the Disassembly property page correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2-5.*

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

All Display Format in SPI3_TX and SPI3_RX

In this option, all valid and invalid data is acquired at the rising edge of the data clock and displayed.

Packet Display Format in SPI3_TX and SPI3_RX

In this option, all valid packet data is acquired at the rising edge of the data clock and displayed.

All Display Format in SPI4 and SPI4_LVTTL

In this option, all the decoded information is displayed. Figure 2–1 shows an example of the All display format for the SPI4 support package.

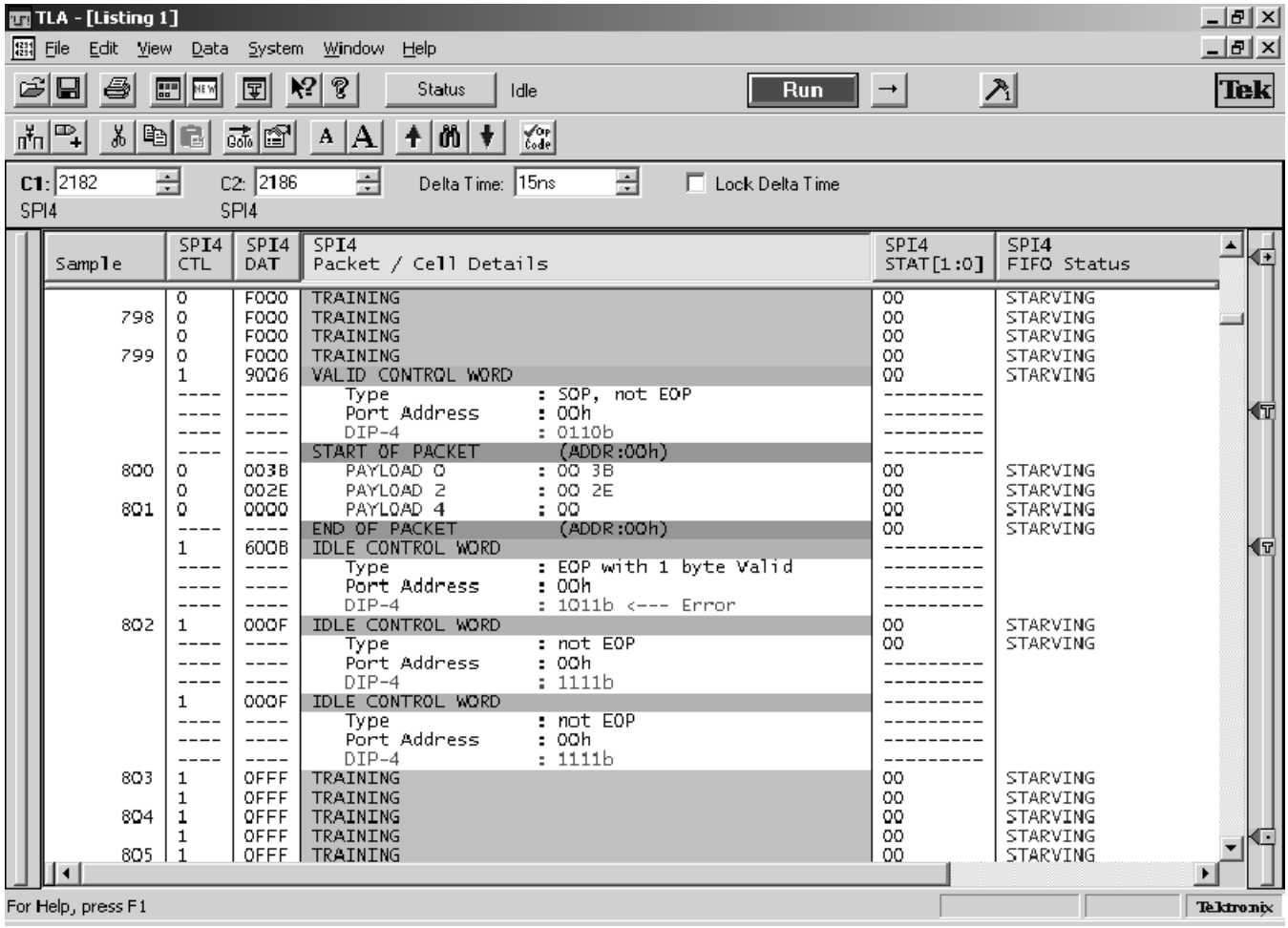


Figure 2–1: Example of All display format for the SPI4 support package

Packet & Control Display Format in SPI4 and SPI4_LVTTL

In this option, the information related to packets and control words, are decoded and displayed. Training related information is not shown.

Figure 2–2 shows an example of the Packet & Control display format for the SPI4 support package.

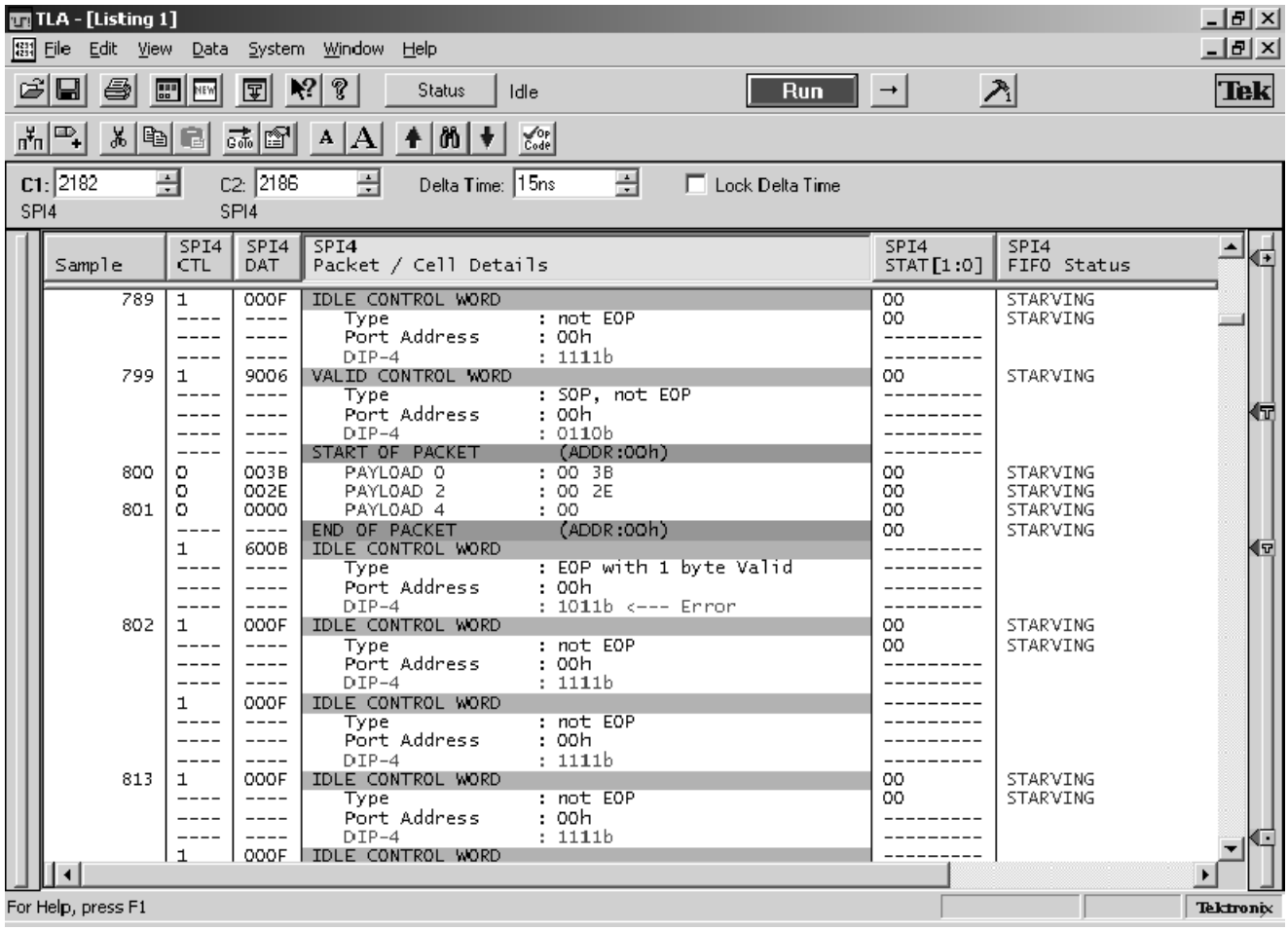


Figure 2–2: Example of Packet & Control display format for the SPI4 support package

Packet Only Display Format in SPI4 and SPI4_LVTTL

In this option, the information related to only packets are decoded and displayed. Other information related to control words is not displayed.

Figure 2–3 shows an example of the Packets Only display format for the SPI4 support package.

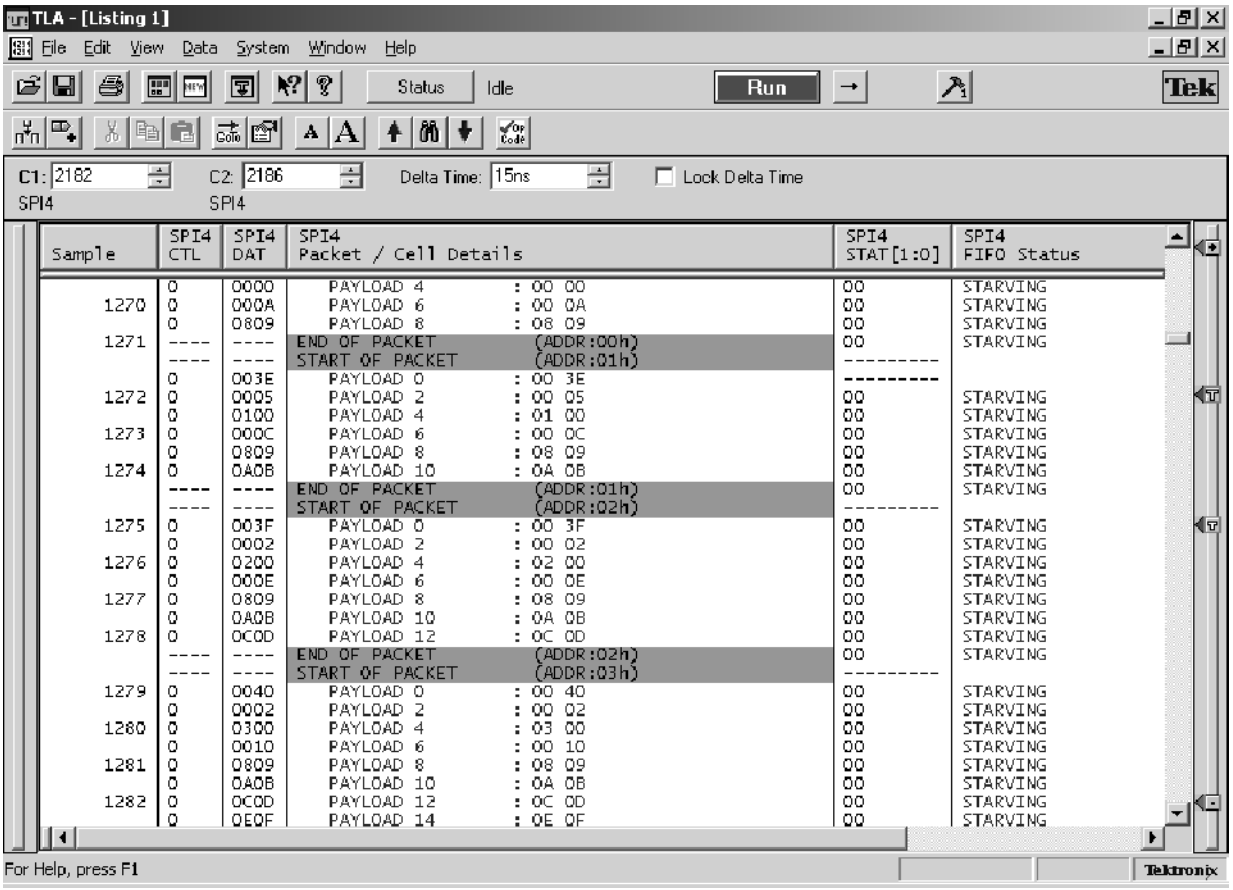


Figure 2–3: Example of Packet Only display format for the SPI4 support package

Trigger Programs

This section describes how to load trigger programs for SPI-3 and SPI-4.2 transmit and receive interfaces. The SPI3_TX, SPI3_RX, SPI4 and SPI4_LVTTL support packages contain a library of EasyTrigger programs enabling you to quickly trigger and qualify common aspects of the SPI-3 and SPI-4.2 bus protocol.

The TCS101 product installs the trigger programs for each support package in the following paths:

C:\ProgramFiles\TLA700\Supports\SPI3_TX\EasyTriggers
C:\ProgramFiles\TLA700\Supports\SPI3_RX\EasyTriggers
C:\ProgramFiles\TLA700\Supports\SPI4\EasyTriggers
C:\ProgramFiles\TLA700\Supports\SPI4_LVTTL\EasyTriggers

Loading Trigger Programs

To load a trigger program from any of the support packages, follow these steps:

1. Load the support package.
2. From the system window, click the 

Trigger button.
3. Click on the "EasyTrigger" tab. Scroll through the EasyTrigger window to find the trigger programs that you need.
4. Select an EasyTrigger program from the list and fill in the fields.

You are now ready to trigger on the acquired data. For more information, refer to the logic analyzer online help and the logic analyzer user manual.

SPI-3 Trigger Programs

The following list of EasyTrigger programs is common for the SPI3_TX and SPI3_RX support packages and can be used independently. The trigger programs are:

Trigger on control condition
Trigger on packet
Trigger on packet from a specific port

SPI-4.2 Trigger Programs

The following list of EasyTrigger programs is common for the SPI4 and SPI4_LVTTL support packages and can be used independently. The trigger programs are:

Trigger on control word
Trigger on a generic packet

SPI-4.2 Setup/Hold Time Adjustments

Some devices will require an adjustment of the Setup/Hold values in the TLA700 Application to get valid test results. The logic analyzer application provides AutoDeskew to automatically deskew and verify the logic analyzer Setup/Hold window. AutoDeskew can also be used to test Setup/Hold violations of the current setting. For more information on AutoDeskew, refer to the logic analyzer online help.

The Setup/Hold adjustments can be made for each channel. You can use custom clock setups and different Setup/Hold settings for each type of clocking. The AutoDeskew capability to analyze the Setup/Hold violations allows you to test for violations that occur with current Setup/Hold settings. You can automatically convert a test setup to a trigger setup for use with the logic analyzer trigger system. This allows you to determine exactly which channels may be failing the Setup/Hold requirements.

AutoDeskew is preconfigured for the support packages SPI4 and SPI4_LVTTL. Follow these steps to use AutoDeskew:

1. Load the support package and click the AutoDeskew button on the tool bar to open the AutoDeskew window.
2. Click the Define Setup button to display the AutoDeskew Setup dialog.
3. Select Custom under AutoDeskew mode. Based on the loaded support package, the AutoDeskew configurations and settings show different options.
4. Choose the appropriate options for the AutoDeskew configuration and settings.
5. Click the Analyze button to start analysis.
6. After the analysis is complete, the results are displayed.
7. Click the Apply button to apply the analyzed results. You can manually examine the window choices and move the sample point if needed before clicking the Apply button.

Each support has several AutoDeskew configurations based on the clock signal that is used as a source clock for acquisition. Each configuration has several settings corresponding to the channels to be analyzed.

SPI4 Configurations and Settings

You can select the following configurations and settings for the SPI4 support package.

SPI4 AutoDeskew Setup

The following setting is available for SPI4 AutoDeskew:

- Analyze SPI4 Signals

SPI4_LVTTL Configurations and Settings

You can select the following configurations and settings for the SPI4 support package.

SPI4_LVTTL AutoDeskew Setup

The following settings are available for SPI4_LVTTL AutoDeskew:

- Analyze SPI4_LVTTL Status Signals
- Analyze SPI4_LVTTL Data & Control Signals

Reference

Channel Group Definitions

This section lists the channel group definitions for the TCS101 product required for disassembly.

Channel Groups

The software automatically defines channel groups for the support package. Tables 3–1 through 3–3 show the channel groups for the TCS101 product for the SPI3_TX, SPI3_RX, SPI4, and SPI4_LVTTL support packages.

Table 3–1: SPI3_TX channel group names

Group name	Display radix
Address	Hexadecimal
DAT	Hexadecimal
Packet/Cell details	None (disassembly generated text)
Control	Symbol
DTPA	Off
Parity	Symbol (disassembly generated text)
Misc	Hexadecimal
Trig_Control	Off (Trigger Group)
Trig_DAT[7:0]	Off (Trigger Group)
Trig_DAT[31:0]	Off (Trigger Group)
Timestamp	

Table 3–2: SPI3_RX channel group names

Group name	Display radix
DAT	Hexadecimal
Packet/Cell details	None (disassembly generated text)
Control	Symbol
Parity	Symbol (disassembly generated text)
Trig_Control	Off (Trigger Group)
Trig_DAT[7:0]	Off (Trigger Group)
Trig_DAT[31:0]	Off (Trigger Group)
Timestamp	

Table 3-3: SPI4 and SPI4_LVTTL channel group names

Group name	Display radix
$CTL	Off (Calibration Group)
$DAT0	Off (Calibration Group)
$DAT1	Off (Calibration Group)
$DAT2	Off (Calibration Group)
$DAT3	Off (Calibration Group)
$DAT4	Off (Calibration Group)
$DAT5	Off (Calibration Group)
$DAT6	Off (Calibration Group)
$DAT7	Off (Calibration Group)
$DAT8	Off (Calibration Group)
$DAT9	Off (Calibration Group)
$DAT10	Off (Calibration Group)
$DAT11	Off (Calibration Group)
$DAT12	Off (Calibration Group)
$DAT13	Off (Calibration Group)
$DAT14	Off (Calibration Group)
$DAT15	Off (Calibration Group)
$STAT0	Off (Calibration Group)
$STAT1	Off (Calibration Group)
CTL_TYPE_A	Off (EasyTrigger Group)
CTL_TYPE_B	Off (EasyTrigger Group)
CTL_TYPE_AB	Off (EasyTrigger Group)
DAT_PORT_A	Off (EasyTrigger Group)
DAT_PORT_B	Off (EasyTrigger Group)
DAT_AB	Off (EasyTrigger Group)
DAT_BA	Off (EasyTrigger Group)
DAT_A	Off (EasyTrigger Group)
DAT_B	Off (EasyTrigger Group)
CTL[1:0]	Off
DATA	Off
STAT	Off
STAT_A	Off
STAT_B	Off
CTL	Binary (Numeric group generated by disassembly)

Table 3-3: SPI4 and SPI4_LVTTL channel group names (Cont.)

Group name	Display radix
DAT	Hexadecimal (Numeric group generated by disassembly)
Packet/Cell Details	None (disassembly generated text)
STAT[1:0]	Binary (disassembly generated text)
FIFO Status	None (disassembly generated text)
Timestamp	

***NOTE**. The groups $STAT0 and $STAT1 are used only in the SPI4 support package.*

Symbol and Channel Assignment Tables

This section lists the symbol tables, channel assignment tables for disassembly and timing, and signal acquisition for each of the support packages.

Symbol Tables

The TCS101 product supplies three symbol table files for the SPI3_TX and SPI3_RX supports and one each for SPI4 and SPI4_LVTTL support packages.

Tables 3–4 through 3–10 show the definitions for the symbol, bit pattern, and meaning of the group symbols in the control symbol tables. The symbol table file for SPI3_TX support package is SPI3_TX_Ctrl.

Table 3-4: SPI3_TX_Ctrl group symbol table definitions

Symbol	Ctrl group value TSX TENB TSOP TEOP TERR TPRTY TMOD1 TMOD0	Description
DATA	0 0 0 0 X X X X	Valid data on TDAT bus
EOP	0 0 0 1 0 X X X	Sample at which TEOP is asserted
SOP	0 0 1 0 X X X X	Sample at which TSOP is asserted
ERROR	0 0 X 1 1 X X X	Erroneous packet transmitted over TDAT bus
PORT_ADDRESS	1 1 0 0 X X X X	Physical port address
SOP&EOP	X 0 1 1 X X X X	Sample at which TSOP and TEOP are asserted

***NOTE**. Binary values are displayed for those control group words that do not have any symbols assigned to them.*

Table 3–5 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the EasyTrigger symbol table for the SPI3_TX support package. The EasyTrigger symbol table file name SPI3_TX_Trig_Ctrl.

Table 3-5: SPI3_TX_Trig_Ctrl group symbol table definitions

Symbol	Trig_Control group value TSOP TEOP TERR	Description
Any control	X X X	-
SOP	1 X X	Start of packet
EOP	X 1 X	End of packet
ERROR	X 1 1	Erroneous packet

Table 3–6 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the Parity symbol table for the SPI3_TX support package. The Parity symbol table file name SPI3_TX_Parity.

Table 3-6: SPI3_TX Parity group symbol table definitions

Symbol	Parity group value TPRTY	Description
Parity_0	0	Parity signal is low
Parity_1	1	Parity signal is high

The symbol table file for SPI3_RX support package is SPI3_RX_Ctrl.

Table 3-7: SPI3_RX_Ctrl group symbol table definitions

Symbol	Ctrl group value RSX RVAL RENB RSOP	 REOP RERR RPRTY RMOD1	 RMOD0	Description
DATA	0 1 X 0	0 X X X	X	Valid data on RDAT bus
SOP	0 1 X 1	0 X X X	X	Sample at which RSOP is asserted
PORT_ADDRESS	1 0 X 0	0 X X X	X	Physical port address

Table 3-7: SPI3_RX_Ctrl group symbol table definitions (Cont.)

Symbol	Ctrl group value RSX RVAL RENB RSOP REOP RERR RPRTY RMOD1 RMOD0	Description
EOP	0 1 X 0 1 0 X X X	Sample at which REOP is asserted
ERROR	0 1 X X 1 1 X X X	Erroneous packet received over RDAT bus
SOP&EOP	X 1 X 1 1 X X X X	Sample at which RSOP and REOP are asserted

***NOTE**. Binary values are displayed for those control group words that do not have any symbols assigned to them.*

Table 3–8 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the EasyTrigger symbol table for the SPI3_RX support package. The EasyTrigger symbol table file name SPI3_RX_Trig_Ctrl.

Table 3-8: SPI3_RX_Trig_Ctrl group symbol table definitions

Symbol	Trig_Control group value RSOP REOP RERR	Description
Any control	X X X	
SOP	1 X X	Start of packet
EOP	X 1 X	End of packet
ERROR	X 1 1	Erroneous packet

Table 3–9 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the Parity symbol table for the SPI3_RX support package. The Parity symbol table file name SPI3_RX_Parity.

Table 3-9: SPI3_RX Parity group symbol table definitions

Symbol	Parity group value	Description
	RPRTY	
Parity_0	0	Parity signal is low
Parity_1	1	Parity signal is high

Table 3–10 shows the definitions for the symbol, bit pattern, and meaning of the group symbols in the control symbol table for the SPI4 and SPI4_LVTTL support packages. The symbol table file for SPI4 and SPI4_LVTTL support packages is SPI4_Ctrl and SPI4_LVTTL_Ctrl. Use these symbols for triggering packet and control word information. By default, the group is off.

Table 3-10: SPI4_Ctrl/SPI4_LVTTL_Ctrl group symbol table definitions

Symbol	Ctrl group value	Description
	CTL_DM/CTL DAT15/DAT31 DAT14/DAT30 DAT13/DAT29 DAT12/DAT28	
(Any_Word)	1 X X X X	-
(Generic_SOP)	1 1 0 X 1	Packet start
(Generic_EOP)	1 X 1 X X	Packet end
(Generic_Abort)	1 X 0 1 X	Packet end abort
0: Idle, not_EOP, training_control	1 0 0 0 0	Training control word
1: Reserved	1 0 0 0 1	Reserved
2: Idle, Abort_last_packet	1 0 0 1 0	Idle control word, abort
3: Reserved	1 0 0 1 1	Reserved
4: Idle, EOP_with_2_bytes_valid	1 0 1 0 0	Idle control word, EOP, both the bytes valid
5: Reserved	1 0 1 0 1	Reserved
6: Idle, EOP_with_1_byte_valid	1 0 1 1 0	Idle control word, EOP, one byte valid
7: Reserved	1 0 1 1 1	Reserved
8: Valid, no_SOP, no_EOP	1 1 0 0 0	Valid packet, not SOP and EOP

Table 3-10: SPI4_Ctrl/SPI4_LVTTL_Ctrl group symbol table definitions (Cont.)

Symbol	Ctrl group value (CTL_DM/CTL DAT15/DAT31 DAT14/DAT30 DAT13/DAT29 DAT12/DAT28)	Description
9: Valid, SOP, no_EOP	1 1 0 0 1	Valid packet, SOP and not EOP
A: Valid, no_SOP, abort	1 1 0 1 0	Valid packet, not SOP and abort
B: Valid, SOP, abort	1 1 0 1 1	Valid packet, SOP and abort
C: Valid, no_SOP, EOP_w/2_bytes_valid	1 1 1 0 0	Valid packet, not SOP and EOP with both the bytes valid
D: Valid, SOP, EOP_w/2_bytes_valid	1 1 1 0 1	Valid packet, SOP and EOP with both the bytes valid
E: Valid, no_SOP, EOP_w/1_byte_valid	1 1 1 1 0	Valid packet, not SOP and EOP with one byte valid
F: Valid, SOP, EOP_w/1_byte_valid	1 1 1 1 1	Valid packet, SOP and EOP with one byte valid

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically.

Channel Assignment Tables

Channel assignments shown in Table 3–11 through Table 3–68 use the following conventions:

- All signals are required by the support package, unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules, unless otherwise noted.
- Any SPI-3 signal ending with the letter “B” indicates that the signal is asserted low.

SPI3_TX Channel Group Assignments

Tables 3–11 through 3–18 show the channel assignments for the logic analyzer groups for the SPI3_TX support package and the bus signal to which each channel connects.

Table 3-11 shows the probe section and channel assignments for the Address group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-11: Address group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
1 (MSB)	C3:7	TADR1
0	C3:6	TADR0

Table 3-12 shows the probe section and channel assignments for the DAT group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-12: DAT group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
31 (MSB)	D1:7	TDAT31
30	D1:6	TDAT30
29	D1:5	TDAT29
28	D1:4	TDAT28
27	D1:3	TDAT27
26	D1:2	TDAT26
25	D1:1	TDAT25
24	D1:0	TDAT24
23	D0:7	TDAT23
22	D0:6	TDAT22
21	D0:5	TDAT21
20	D0:4	TDAT20
19	D0:3	TDAT19
18	D0:2	TDAT18
17	D0:1	TDAT17
16	D0:0	TDAT16
15	A1:7	TDAT15
14	A1:6	TDAT14
13	A1:5	TDAT13
12	A1:4	TDAT12

Table 3-12: DAT group assignments for SPI3_TX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
11	A1:3	TDAT11
10	A1:2	TDAT10
9	A1:1	TDAT9
8	A1:0	TDAT8
7	A0:7	TDAT7
6	A0:6	TDAT6
5	A0:5	TDAT5
4	A0:4	TDAT4
3	A0:3	TDAT3
2	A0:2	TDAT2
1	A0:1	TDAT1
0 (LSB)	A0:0	TDAT0

Table 3–13 shows the probe section and channel assignments for the Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is SPI3_TX_Ctrl.

Table 3-13: Control group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
7 (MSB)	C2:3	TSX
6	C2:2	TENB
5	C2:0	TSOP
4	C2:1	TEOP
3	C3:1	TERR
2	C3:3	TPRTY
1	C3:5	TMOD1
0 (LSB)	C3:4	TMOD0

Table 3–14 shows the probe section and channel assignments for the DTPA group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-14: DTPA group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
3 (MSB)	C2:7	DTPA3
2	C2:6	DTPA2
1	C2:5	DTPA1
0 (LSB)	C2:4	DTPA0

Table 3–15 shows the probe section and channel assignments for the Misc group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-15: Misc group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
1 (MSB)	C3:2	PTPA
0	C3:0	STPA

Table 3–16 shows the probe section and channel assignments for the Trig_Control group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-16: Trig_Control group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
2 (MSB)	C2:0	TSOP
1	C2:1	TEOP
0 (LSB)	C3:1	TERR

Table 3–17 shows the probe section and channel assignments for the Trig_DAT[7:0] group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-17: Trig_DAT[7:0] group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
7 (MSB)	A0:7	TDAT7
6	A0:6	TDAT6
5	A0:5	TDAT5
4	A0:4	TDAT4
3	A0:3	TDAT3
2	A0:2	TDAT2
1	A0:1	TDAT1
0 (LSB)	A0:0	TDAT0

Table 3–18 shows the probe section and channel assignments for the Trig_DAT[31:0] group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-18: Trig_DAT[31:0] group assignments for SPI3_TX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
31 (MSB)	D1:7	TDAT31
30	D1:6	TDAT30
29	D1:5	TDAT29
28	D1:4	TDAT28
27	D1:3	TDAT27
26	D1:2	TDAT26
25	D1:1	TDAT25
24	D1:0	TDAT24
23	D0:7	TDAT23
22	D0:6	TDAT22
21	D0:5	TDAT21
20	D0:4	TDAT20
19	D0:3	TDAT19
18	D0:2	TDAT18

Table 3-18: Trig_DAT[31:0] group assignments for SPI3_TX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
17	D0:1	TDAT17
16	D0:0	TDAT16
15	A1:7	TDAT15
14	A1:6	TDAT14
13	A1:5	TDAT13
12	A1:4	TDAT12
11	A1:3	TDAT11
10	A1:2	TDAT10
9	A1:1	TDAT9
8	A1:0	TDAT8
7	A0:7	TDAT7
6	A0:6	TDAT6
5	A0:5	TDAT5
4	A0:4	TDAT4
3	A0:3	TDAT3
2	A0:2	TDAT2
1	A0:1	TDAT1
0 (LSB)	A0:0	TDAT0

SPI3_RX Channel Group Assignments

Tables 3–19 through 3–23 show the channel assignments for the logic analyzer groups for the SPI3_RX support package and the bus signal to which each channel connects.

Table 3–19 shows the probe section and channel assignments for the DAT group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-19: DAT group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 receive signal name
31 (MSB)	D1:7	RDAT31
30	D1:6	RDAT30
29	D1:5	RDAT29
28	D1:4	RDAT28

Table 3-19: DAT group assignments for SPI3_RX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 receive signal name
27	D1:3	RDAT27
26	D1:2	RDAT26
25	D1:1	RDAT25
24	D1:0	RDAT24
23	D0:7	RDAT23
22	D0:6	RDAT22
21	D0:5	RDAT21
20	D0:4	RDAT20
19	D0:3	RDAT19
18	D0:2	RDAT18
17	D0:1	RDAT17
16	D0:0	RDAT16
15	A1:7	RDAT15
14	A1:6	RDAT14
13	A1:5	RDAT13
12	A1:4	RDAT12
11	A1:3	RDAT11
10	A1:2	RDAT10
9	A1:1	RDAT9
8	A1:0	RDAT8
7	A0:7	RDAT7
6	A0:6	RDAT6
5	A0:5	RDAT5
4	A0:4	RDAT4
3	A0:3	RDAT3
2	A0:2	RDAT2
1	A0:1	RDAT1
0 (LSB)	A0:0	RDAT0

Table 3–20 shows the probe section and channel assignments for the Control group and the bus signal to which each channel connects. By default, this channel group is displayed in symbols. The symbol table file name is SPI3_RX_Ctrl.

Table 3-20: Control group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 receive signal name
8	C2:3	RSX
7	Clock:1	RVAL
6	C2:2	RENB
5	C2:0	RSOP
4	C2:1	REOP
3	C3:1	RERR
2	C3:3	RPRTY
1	C3:5	RMOD1
0 (LSB)	C3:4	RMOD0

Table 3–21 shows the probe section and channel assignments for the Trig_Control group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-21: Trig_Control group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
2 (MSB)	C2:0	RSOP
1	C2:1	REOP
0 (LSB)	C3:1	RERR

Table 3–22 shows the probe section and channel assignments for the Trig_DAT[7:0] group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-22: Trig_DAT[7:0] group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
7 (MSB)	A0:7	RDAT7
6	A0:6	RDAT6

Table 3-22: Trig_DAT[7:0] group assignments for SPI3_RX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
5	A0:5	RDAT5
4	A0:4	RDAT4
3	A0:3	RDAT3
2	A0:2	RDAT2
1	A0:1	RDAT1
0 (LSB)	A0:0	RDAT0

Table 3–23 shows the probe section and channel assignments for the Trig_DAT[31:0] group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-23: Trig_DAT[31:0] group assignments for SPI3_RX support package

Bit order	Logic analyzer channel	SPI-3 transmit signal name
31 (MSB)	D1:7	RDAT31
30	D1:6	RDAT30
29	D1:5	RDAT29
28	D1:4	RDAT28
27	D1:3	RDAT27
26	D1:2	RDAT26
25	D1:1	RDAT25
24	D1:0	RDAT24
23	D0:7	RDAT23
22	D0:6	RDAT22
21	D0:5	RDAT21
20	D0:4	RDAT20
19	D0:3	RDAT19
18	D0:2	RDAT18
17	D0:1	RDAT17
16	D0:0	RDAT16
15	A1:7	RDAT15
14	A1:6	RDAT14

Table 3-23: Trig_DAT[31:0] group assignments for SPI3_RX support package (Cont.)

Bit order	Logic analyzer channel	SPI-3 transmit signal name
13	A1:5	RDAT13
12	A1:4	RDAT12
11	A1:3	RDAT11
10	A1:2	RDAT10
9	A1:1	RDAT9
8	A1:0	RDAT8
7	A0:7	RDAT7
6	A0:6	RDAT6
5	A0:5	RDAT5
4	A0:4	RDAT4
3	A0:3	RDAT3
2	A0:2	RDAT2
1	A0:1	RDAT1
0 (LSB)	A0:0	RDAT0

SPI4 and SPI4_LVTTL Channel Group Assignments

The SPI-4.2 supports are common to both the SPI-4.2 Transmit and Receive buses. Therefore:

- TDAT and RDAT are referred to as DAT
- TCTL and RCTL are referred to as CTL
- TSCLK and RSCLK are referred to as SCLK
- TDCLK and RDCLK are referred to as DCLK

When you use the SPI4 and SPI4_LVTTL supports, do not connect the following logic analyzer channels to any signals because they are demuxed.

Qual:0
D3:7-0
D1:7-0
C1:7
C1:6

Tables 3–24 through 3–49 show the channel assignments for the groups of the SPI4 and SPI4_LVTTL support packages and the bus signal to which each channel connects.

Table 3–24 shows the probe section and channel assignments for the $CTL group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-24: $CTL group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	Clock:1	CTL
0	Qual:0	CTL_DM

Table 3–25 shows the probe section and channel assignments for the $DAT0 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-25: $DAT0 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:0	DAT0
0	D3:0	DAT16

Table 3–26 shows the probe section and channel assignments for the $DAT1 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-26: $DAT1 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:1	DAT1
0	D3:1	DAT17

Table 3–27 shows the probe section and channel assignments for the $DAT2 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-27: $DAT2 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:2	DAT2
0	D3:2	DAT18

Table 3–28 shows the probe section and channel assignments for the $DAT3 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-28: $DAT3 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:3	DAT3
0	D3:3	DAT19

Table 3–29 shows the probe section and channel assignments for the $DAT4 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-29: $DAT4 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:4	DAT4
0	D3:4	DAT20

Table 3–30 shows the probe section and channel assignments for the $DAT5 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-30: $DAT5 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:5	DAT5
0	D3:5	DAT21

Table 3–31 shows the probe section and channel assignments for the $DAT6 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-31: $DAT6 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:6	DAT6
0	D3:6	DAT22

Table 3–32 shows the probe section and channel assignments for the $DAT7 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-32: $DAT7 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A3:7	DAT7
0	D3:7	DAT23

Table 3–33 shows the probe section and channel assignments for the $DAT8 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-33: $DAT8 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:0	DAT8
0	D1:0	DAT24

Table 3–34 shows the probe section and channel assignments for the $DAT9 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-34: $DAT9 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:1	DAT9
0	D1:1	DAT25

Table 3–35 shows the probe section and channel assignments for the $DAT10 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-35: $DAT10 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:2	DAT10
0	D1:2	DAT26

Table 3–36 shows the probe section and channel assignments for the $DAT11 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-36: $DAT11 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:3	DAT11
0	D1:3	DAT27

Table 3–37 shows the probe section and channel assignments for the $DAT12 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-37: $DAT12 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:4	DAT12
0	D1:4	DAT28

Table 3–38 shows the probe section and channel assignments for the $DAT13 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-38: $DAT13 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:5	DAT13
0	D1:5	DAT29

Table 3–39 shows the probe section and channel assignments for the $DAT14 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-39: $DAT14 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:6	DAT14
0	D1:6	DAT30

Table 3–40 shows the probe section and channel assignments for the $DAT15 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-40: $DAT15 group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	A1:7	DAT15
0	D1:7	DAT31

Table 3–41 shows the probe section and channel assignments for the $STAT0 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-41: $STAT0 group assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1 (MSB)	C3:6	STAT0
0	C1:6	STAT0_DM

Table 3–42 shows the probe section and channel assignments for the $STAT1 group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-42: $STAT1 group assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1 (MSB)	C3:7	STAT1
0	C1:7	STAT1_DM

***NOTE**. The groups $STAT0 and $STAT1 are used only in the SPI4 support package.*

Table 3–43 shows the probe section and channel assignments for the DATA group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-43: DATA group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
31 (MSB)	A1:7	DAT15
30	A1:6	DAT14
29	A1:5	DAT13
28	A1:4	DAT12
27	A1:3	DAT11
26	A1:2	DAT10

Table 3-43: DATA group assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
25	A1:1	DAT9
24	A1:0	DAT8
23	A3:7	DAT7
22	A3:6	DAT6
21	A3:5	DAT5
20	A3:4	DAT4
19	A3:3	DAT3
18	A3:2	DAT2
17	A3:1	DAT1
16	A3:0	DAT0
15	D1:7	DAT31
14	D1:6	DAT30
13	D1:5	DAT29
12	D1:4	DAT28
11	D1:3	DAT27
10	D1:2	DAT26
9	D1:1	DAT25
8	D1:0	DAT24
7	D3:7	DAT23
6	D3:6	DAT22
5	D3:5	DAT21
4	D3:4	DAT20
3	D3:3	DAT19
2	D3:2	DAT18
1	D3:1	DAT17
0 (LSB)	D3:0	DAT16

Table 3–44 shows the probe section and channel assignments for the CTL[1:0] group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-44: CTL[1:0] group assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
1 (MSB)	Qual:0	CTL_DM
0	Clock:1	CTL

Table 3–45 shows the probe section and channel assignments for the STAT group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-45: STAT group channel assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
3 (MSB)	C3:7	STAT1
2	C3:6	STAT0
1	C1:7	STAT1_DM
0 (LSB)	C1:6	STAT0_DM

Table 3–46 shows the probe section and channel assignments for the STAT group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-46: STAT group channel assignments for SPI4_LVTTL support package

Bit order	Logic analyzer channel	SPI4_LVTTL support package signal name
1 (MSB)	C3:7	STAT1
0	C3:6	STAT0

Table 3–47 shows the probe section and channel assignments for the STAT_A group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-47: STAT_A group channel assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1 (MSB)	C3:7	STAT1
0	C3:6	STAT0

Table 3–48 shows the probe section and channel assignments for the STAT_B group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-48: STAT_B group channel assignments for SPI4 support package

Bit order	Logic analyzer channel	SPI4 support package signal name
1	C1:7	STAT1_DM
0	C1:6	STAT0_DM

NOTE*. The groups STAT_A and $STAT_B are used only in the SPI4 support package.*

Table 3–49 shows the probe section and channel assignments for the SCLK group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-49: SCLK group channel assignments for SPI4_LVTTL support package

Bit order	Logic analyzer channel	SPI4_LVTTL support package signal name
1	Clock:3	SCLK

EasyTrigger Channel Assignments

Tables 3–50 through 3–58 show the EasyTrigger channel assignments for the groups and the bus signal to which each channel connects. These groups are common for both SPI4 and SPI4_LVTTL support packages.

Table 3–50 shows the probe section and channel assignments for the CTL_TYPE_A group and the bus signal to which each channel connects. By default, this channel group is off. The symbol tables SPI4_Ctrl and SPI4_LVTTL_Ctrl are associated with this group.

Table 3-50: CTL_TYPE_A group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
4 (MSB)	Clock:1	CTL
3	A1:7	DAT15
2	A1:6	DAT14
1	A1:5	DAT13
0 (LSB)	A1:4	DAT12

Table 3–51 shows the probe section and channel assignments for the CTL_TYPE_B group and the bus signal to which each channel connects. By default, this channel group is off. The symbol tables SPI4_Ctrl and SPI4_LVTTL_Ctrl are associated with this group.

Table 3-51: CTL_TYPE_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
4 (MSB)	Qual:0	CTL_DM
3	D1:7	DAT31
2	D1:6	DAT30
1	D1:5	DAT29
0 (LSB)	D1:4	DAT28

Table 3–52 shows the probe section and channel assignments for the CTL_TYPE_AB group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-52: CTL_TYPE_AB group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
9 (MSB)	Clock:1	CTL
8	A1:7	DAT15
7	A1:6	DAT14
6	A1:5	DAT13
5	A1:4	DAT12
4	Qual:0	CTL_DM
3	D1:7	DAT31
2	D1:6	DAT30
1	D1:5	DAT29
0 (LSB)	D1:4	DAT28

Table 3–53 shows the probe section and channel assignments for the DAT_PORT_A group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-53: DAT_PORT_A group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
7 (MSB)	A1:3	DAT11
6	A1:2	DAT10
5	A3:1	DAT9
4	A3:0	DAT8
3	A3:7	DAT7
2	A3:6	DAT6
1	A3:5	DAT5
0 (LSB)	A3:4	DAT4

Table 3–54 shows the probe section and channel assignments for the DAT_PORT_B group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-54: DAT_PORT_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
7 (MSB)	D1:3	DAT27
6	D1:2	DAT26
5	D1:1	DAT25
4	D1:0	DAT24
3	D3:7	DAT23
2	D3:6	DAT22
1	D3:5	DAT21
0 (LSB)	D3:4	DAT20

Table 3–55 shows the probe section and channel assignments for the DAT_AB group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-55: DAT_AB group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
31 (MSB)	A1:7	DAT15
30	A1:6	DAT14
29	A1:5	DAT13
28	A1:4	DAT12
27	A1:3	DAT11
26	A1:2	DAT10
25	A1:1	DAT9
24	A1:0	DAT8
23	A3:7	DAT7
22	A3:6	DAT6
21	A3:5	DAT5
20	A3:4	DAT4

Table 3-55: DAT_AB group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
19	A3:3	DAT3
18	A3:2	DAT2
17	A3:1	DAT1
16	A3:0	DAT0
15	D1:7	DAT31
14	D1:6	DAT30
13	D1:5	DAT29
12	D1:4	DAT28
11	D1:3	DAT27
10	D1:2	DAT26
9	D1:1	DAT25
8	D1:0	DAT24
7	D3:7	DAT23
6	D3:6	DAT22
5	D3:5	DAT21
4	D3:4	DAT20
3	D3:3	DAT19
2	D3:2	DAT18
1	D3:1	DAT17
0 (LSB)	D3:0	DAT16

Table 3–56 shows the probe section and channel assignments for the DAT_BA group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-56: DAT_BA group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
31 (MSB)	D1:7	DAT31
30	D1:6	DAT30
29	D1:5	DAT29

Table 3-56: DAT_BA group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
28	D1:4	DAT28
27	D1:3	DAT27
26	D1:2	DAT26
25	D1:1	DAT25
24	D1:0	DAT24
23	D3:7	DAT23
22	D3:6	DAT22
21	D3:5	DAT21
20	D3:4	DAT20
19	D3:3	DAT19
18	D3:2	DAT18
17	D3:1	DAT17
16	D3:0	DAT16
15	A1:7	DAT15
14	A1:6	DAT14
13	A1:5	DAT13
12	A1:4	DAT12
11	A1:3	DAT11
10	A1:2	DAT10
9	A1:1	DAT9
8	A1:0	DAT8
7	A3:7	DAT7
6	A3:6	DAT6
5	A3:5	DAT5
4	A3:4	DAT4
3	A3:3	DAT3
2	A3:2	DAT2
1	A3:1	DAT1
0 (LSB)	A3:0	DAT0

Table 3–57 shows the probe section and channel assignments for the DAT_A group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-57: DAT_A group channel EasyTrigger assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
15 (MSB)	A1:7	DAT15
14	A1:6	DAT14
13	A1:5	DAT13
12	A1:4	DAT12
11	A1:3	DAT11
10	A1:2	DAT10
9	A1:1	DAT9
8	A1:0	DAT8
7	A3:7	DAT7
6	A3:6	DAT6
5	A3:5	DAT5
4	A3:4	DAT4
3	A3:3	DAT3
2	A3:2	DAT2
1	A3:1	DAT1
0 (LSB)	A3:0	DAT0

Table 3–58 shows the probe section and channel assignments for the DAT_B group and the bus signal to which each channel connects. By default, this channel group is off.

Table 3-58: DAT_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
15 (MSB)	D1:7	DAT31
14	D1:6	DAT30
13	D1:5	DAT29
12	D1:4	DAT28

Table 3-58: DAT_B group EasyTrigger channel assignments for SPI4 and SPI4_LVTTL support packages (Cont.)

Bit order	Logic analyzer channel	SPI4/SPI4_LVTTL support package signal name
11	D1:3	DAT27
10	D1:2	DAT26
9	D1:1	DAT25
8	D1:0	DAT24
7	D3:7	DAT23
6	D3:6	DAT22
5	D3:5	DAT21
4	D3:4	DAT20
3	D3:3	DAT19
2	D3:2	DAT18
1	D3:1	DAT17
0 (LSB)	D3:0	DAT16

Clock and Qualifier Channel Assignments

Tables 3–59 through 3–60 show the channel assignments for the clock and qualifier probes for the SPI3_TX interface, and the bus signal to which each channel connects.

Table 3-59: Clock channel assignments for SPI3_TX support package

Logic analyzer channel	SPI-3 transmit signal name
Clock:3	TFCLK

Table 3-60: Qualifier channel assignments for SPI3_TX support package

Logic analyzer channel	SPI-3 transmit signal name
C2:3	TSX
C2:2	TENB

Tables 3-61 through 3-62 show the channel assignments for the clock and qualifier probes for the SPI3_RX interface, and the bus signal to which each channel connects.

Table 3-61: Clock channel assignments for SPI3_RX support package

Logic analyzer channel	SPI-3 receive signal name
Clock:3	RFCLK

Table 3-62: Qualifier channel assignments for SPI3_RX support package

Logic analyzer channel	SPI-3 receive signal name
C2:3	RSX
C2:2	RENB
Clock:1	RVAL

Table 3-63 shows the channel assignments for the clock and qualifier probes for the SPI4 support, and the bus signal to which each channel connects.

Table 3-63: Clock and qualifier channel assignments for SPI4 support package

Logic analyzer channel	SPI4 support package signal name
Clock:0	DCLK

Table 3-64 shows the channel assignments for the clock and qualifier probes for the SPI4_LVTTL support, and the bus signal to which each channel connects.

Table 3-64: Clock and qualifier channel assignments for SPI4_LVTTL support package

Logic analyzer channel	SPI4_LVTTL support package signal name
Clock:0	DCLK
Clock:3	SCLK

Signals Required for Clocking and Disassembly

Tables 3–65 through 3–66 show the signals required for clocking and disassembly for the TCS101 product.

SPI-3 Signals. Tables 3–65 through 3–66 show the signals and logic analyzer channels required for clocking and disassembly of SPI3 transmit and receive interfaces.

Table 3-65: SPI-3 transmit signals required for clocking and disassembly

Logic analyzer channel	SPI-3 transmit signal/group name
Clock:3	TFCLK
C2:3-0, C3:1, C3:3, C3:4-5	Control group
A1, A0, D1, D0	DAT group
C2:7-4	DTPA group
C3:6-7	Address group
C3:2, C3:0	Misc

Table 3-66: SPI-3 receive signals required for clocking and disassembly

Logic analyzer channel	SPI-3 transmit signal/group name
Clock:3	RFCLK
C2:3-0, Clock:1, C3:1, C3:3, C3:4-5	Control group
A1, A0, D1, D0	DAT group

SPI-4.2 Signals. Tables 3–67 and 3–68 show the signals and logic analyzer channels required for clocking and disassembly of SPI4 and SPI4_LVTTL support packages.

Table 3-67: SPI-4.2 signals required for clocking and disassembly for SPI4 support package

Logic analyzer channel	SPI4 support package signal name
Clock:0	DCLK
Clock:1	CTL

Table 3-67: SPI-4.2 signals required for clocking and disassembly for SPI4 support package (Cont.)

Logic analyzer channel	SPI4 support package signal name
A1	DAT15-DAT8
A3	DAT7-DAT0
C3:7	STAT1
C3:6	STAT0

Table 3-68: SPI-4.2 signals required for clocking and disassembly for SPI4_LVTTL support package

Logic analyzer channel	SPI4_LVTTL support package signal name
Clock:0	DCLK
Clock:1	CTL
Clock:3	SCLK
A1	DAT15-DAT8
A3	DAT7-DAT0
C3:7	STAT1
C3:6	STAT0

Signal Source To Probe Connections

For design purposes, you may need to make connections between the Signal Source and the P6880 or the P6860 Logic Analyzer Probe. Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual, Tektronix part number 071-1059-XX, for more information on mechanical specifications. Tables 3–70 through 3–76 show the Signal Source to probe pin connections.

The recommended pin assignment is the AMP pin assignment for the SPI3_TX and SPI3_RX support packages. See Table 3–69.

Table 3-69: Recommended pin assignments for a Mictor connector (component side)

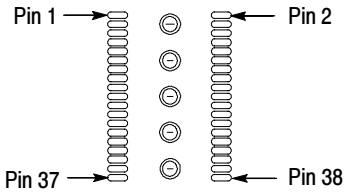
Type of pin assignment	Comments
Recommended  **AMP Pin Assignment**	Recommended. This pin assignment is the industry standard and is what we recommend that you use.

Figure 3-1 shows a sample of P6860 high density probe land footprint.

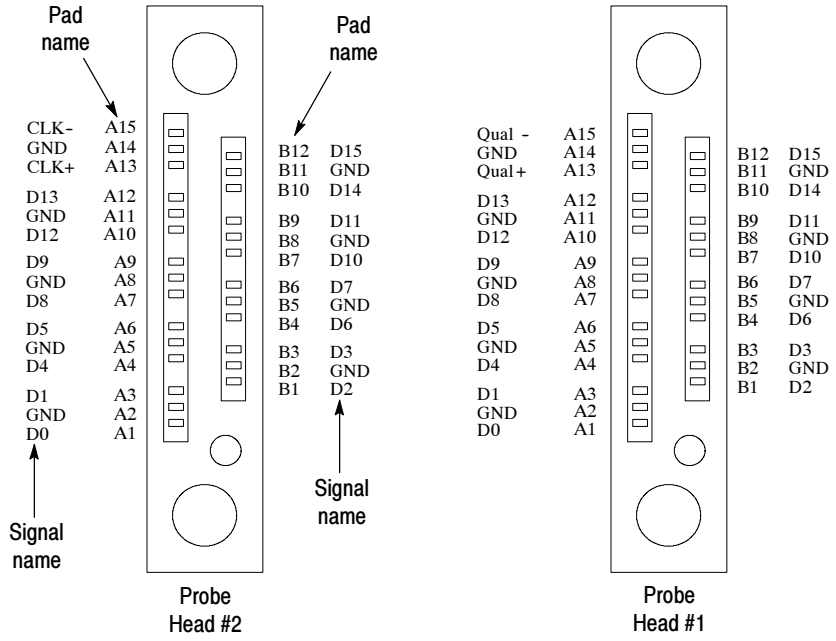


Figure 3-1: Sample of P6860 High-Density probe land footprint

Connections for SPI3_TX Support

Table 3-70 shows the pin connections for the SPI3_TX support package.

Table 3-70: Pin connections for SPI3_TX support package

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
Clock:3	TFCLK	A13	CK3+ Probe#1 probe head 2	Mictor 1 pin 5
-	-	A15*	CK3- Probe#1 probe head 2	-
C2:3	TSX	B3	Data3 Probe#1 probe head 2	Mictor 1 pin 31
C2:2	TENB	B1	Data2 Probe#1 probe head 2	Mictor 1 pin 33
C2:1	TEOP	A3	Data1 Probe#1 probe head 2	Mictor 1 pin 35
C2:0	TSOP	A1	Data0 Probe#1 probe head 2	Mictor 1 pin 37
C2:7	DTPA3	B6	Data7 Probe#1 probe head 2	Mictor 1 pin 23
C2:6	DTPA2	B4	Data6 Probe#1 probe head 2	Mictor 1 pin 25
C2:5	DTPA1	A6	Data5 Probe#1 probe head 2	Mictor 1 pin 27
C2:4	DTPA0	A4	Data4 Probe#1 probe head 2	Mictor 1 pin 29
C3:7	TADR1	B12	Data15 Probe#1 probe head 2	Mictor 1 pin 7

Table 3-70: Pin connections for SPI3_TX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
C3:6	TADR0	B10	Data14 Probe#1 probe head 2	Mictor 1 pin 9
C3:5	TMOD1	A12	Data13 Probe#1 probe head 2	Mictor 1 pin 11
C3:4	TMOD0	A10	Data12 Probe#1 probe head 2	Mictor 1 pin 13
C3:3	TPRTY	B9	Data11 Probe#1 probe head 2	Mictor 1 pin 15
C3:2	PTPA	B7	Data10 Probe#1 probe head 2	Mictor 1 pin 17
C3:1	TERR	A9	Data9 Probe#1 probe head 2	Mictor 1 pin 19
C3:0	STPA	A7	Data8 Probe#1 probe head 2	Mictor 1 pin 21
D1:7	TDAT31	B12	Data15 Probe#2 probe head 1	Mictor 2 pin 7
D1:6	TDAT30	B10	Data14 Probe#2 probe head 1	Mictor 2 pin 9
D1:5	TDAT29	A12	Data13 Probe#2 probe head 1	Mictor 2 pin 11
D1:4	TDAT28	A10	Data12 Probe#2 probe head 1	Mictor 2 pin 13
D1:3	TDAT27	B9	Data11 Probe#2 probe head 1	Mictor 2 pin 15
D1:2	TDAT26	B7	Data10 Probe#2 probe head 1	Mictor 2 pin 17
D1:1	TDAT25	A9	Data9 Probe#2 probe head 1	Mictor 2 pin 19
D1:0	TDAT24	A7	Data8 Probe#2 probe head 1	Mictor 2 pin 21
D0:7	TDAT23	B6	Data7 Probe#2 probe head 1	Mictor 2 pin 23
D0:6	TDAT22	B4	Data6 Probe#2 probe head 1	Mictor 2 pin 25
D0:5	TDAT21	A6	Data5 Probe#2 probe head 1	Mictor 2 pin 27
D0:4	TDAT20	A4	Data4 Probe#2 probe head 1	Mictor 2 pin 29
D0:3	TDAT19	B3	Data3 Probe#2 probe head 1	Mictor 2 pin 31
D0:2	TDAT18	B1	Data2 Probe#2 probe head 1	Mictor 2 pin 33
D0:1	TDAT17	A3	Data1 Probe#2 probe head 1	Mictor 2 pin 35
D0:0	TDAT16	A1	Data0 Probe#2 probe head 1	Mictor 2 pin 37
A1:7	TDAT15	B12	Data15 Probe#2 probe head 2	Mictor 2 pin 8
A1:6	TDAT14	B10	Data14 Probe#2 probe head 2	Mictor 2 pin 10
A1:5	TDAT13	A12	Data13 Probe#2 probe head 2	Mictor 2 pin 12
A1:4	TDAT12	A10	Data12 Probe#2 probe head 2	Mictor 2 pin 14
A1:3	TDAT11	B9	Data11 Probe#2 probe head 2	Mictor 2 pin 16
A1:2	TDAT10	B7	Data10 Probe#2 probe head 2	Mictor 2 pin 18
A1:1	TDAT9	A9	Data9 Probe#2 probe head 2	Mictor 2 pin 20
A1:0	TDAT8	A7	Data8 Probe#2 probe head 2	Mictor 2 pin 22
A0:7	TDAT7	B6	Data7 Probe#2 probe head 2	Mictor 2 pin 24
A0:6	TDAT6	B4	Data6 Probe#2 probe head 2	Mictor 2 pin 26
A0:5	TDAT5	A6	Data5 Probe#2 probe head 2	Mictor 2 pin 28

Table 3-70: Pin connections for SPI3_TX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
A0:4	TDAT4	A4	Data4 Probe#2 probe head 2	Mictor 2 pin 30
A0:3	TDAT3	B3	Data3 Probe#2 probe head 2	Mictor 2 pin 32
A0:2	TDAT2	B1	Data2 Probe#2 probe head 2	Mictor 2 pin 34
A0:1	TDAT1	A3	Data1 Probe#2 probe head 2	Mictor 2 pin 36
A0:0	TDAT0	A1	Data0 Probe#2 probe head 2	Mictor 2 pin 38

* **To be connected to ground in case of P6860 probe**

NOTE. *The logic analyzer module end of the P6434 probe cable has two parts (Pin 1 side and Pin 38 side). Connect the Pin 1 side of the module end to D1 and D0 sections of the logic analyzer module. Connect the Pin 38 side of the module end to A1 and A0 sections of the logic analyzer module.*

Refer to the P6434 Mass Termination Probe instruction manual, Tektronix part number 070-9793-03 to identify the Pin 1 side and the Pin 38 side of the AMP Mictor connector.

For example, the P6434 A probe's module end has two sections — Pin 1 side (A3-A2) and Pin 38 side (A1-A0). You should connect the A3-A2 side of the P6434 module end to D1-D0 of the logic analyzer module and A1-A0 side of the P6434 module end to A1-A0 of the logic analyzer module.

Connections for SPI3_RX Support

Table 3–71 shows the pin connections for the SPI3_RX support package.

Table 3-71: Pin connections for SPI3_RX support package

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
Clock:3	RFCLK	A13	CK3+ Probe#1 probe head 2	Mictor 1 pin 5
-	-	A15*	CK3- Probe#1 probe head 2	-
C2:3	RSX	B3	Data3 Probe#1 probe head 2	Mictor 1 pin 31
C2:2	RENB	B1	Data2 Probe#1 probe head 2	Mictor 1 pin 33
C2:1	REOP	A3	Data1 Probe#1 probe head 2	Mictor 1 pin 35
C2:0	RSOP	A1	Data0 Probe#1 probe head 2	Mictor 1 pin 37
C3:5	RMOD1	A12	Data13 Probe#1 probe head 2	Mictor 1 pin 11
C3:4	RMOD0	A10	Data12 Probe#1 probe head 2	Mictor 1 pin 13

Table 3-71: Pin connections for SPI3_RX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
C3:3	RPRTY	B9	Data11 Probe#1 probe head 2	Mictor 1 pin 15
C3:1	RERR	A9	Data9 Probe#1 probe head 2	Mictor 1 pin 19
D1:7	RDAT31	B12	Data15 Probe#2 probe head 1	Mictor 2 pin 7
D1:6	RDAT30	B10	Data14 Probe#2 probe head 1	Mictor 2 pin 9
D1:5	RDAT29	A12	Data13 Probe#2 probe head 1	Mictor 2 pin 11
D1:4	RDAT28	A10	Data12 Probe#2 probe head 1	Mictor 2 pin 13
D1:3	RDAT27	B9	Data11 Probe#2 probe head 1	Mictor 2 pin 15
D1:2	RDAT26	B7	Data10 Probe#2 probe head 1	Mictor 2 pin 17
D1:1	RDAT25	A9	Data9 Probe#2 probe head 1	Mictor 2 pin 19
D1:0	RDAT24	A7	Data8 Probe#2 probe head 1	Mictor 2 pin 21
D0:7	RDAT23	B6	Data7 Probe#2 probe head 1	Mictor 2 pin 23
D0:6	RDAT22	B4	Data6 Probe#2 probe head 1	Mictor 2 pin 25
D0:5	RDAT21	A6	Data5 Probe#2 probe head 1	Mictor 2 pin 27
D0:4	RDAT20	A4	Data4 Probe#2 probe head 1	Mictor 2 pin 29
D0:3	RDAT19	B3	Data3 Probe#2 probe head 1	Mictor 2 pin 31
D0:2	RDAT18	B1	Data2 Probe#2 probe head 1	Mictor 2 pin 33
D0:1	RDAT17	A3	Data1 Probe#2 probe head 1	Mictor 2 pin 35
D0:0	RDAT16	A1	Data0 Probe#2 probe head 1	Mictor 2 pin 37
Clock:1	RVAL	A13	CK1+ Probe#2 probe head 2	Mictor 2 pin 6
-	-	A15*	CK1- Probe#2 probe head 2	-
A1:7	RDAT15	B12	Data15 Probe#2 probe head 2	Mictor 2 pin 8
A1:6	RDAT14	B10	Data14 Probe#2 probe head 2	Mictor 2 pin 10
A1:5	RDAT13	A12	Data13 Probe#2 probe head 2	Mictor 2 pin 12
A1:4	RDAT12	A10	Data12 Probe#2 probe head 2	Mictor 2 pin 14
A1:3	RDAT11	B9	Data11 Probe#2 probe head 2	Mictor 2 pin 16
A1:2	RDAT10	B7	Data10 Probe#2 probe head 2	Mictor 2 pin 18
A1:1	RDAT9	A9	Data9 Probe#2 probe head 2	Mictor 2 pin 20
A1:0	RDAT8	A7	Data8 Probe#2 probe head 2	Mictor 2 pin 22
A0:7	RDAT7	B6	Data7 Probe#2 probe head 2	Mictor 2 pin 24
A0:6	RDAT6	B4	Data6 Probe#2 probe head 2	Mictor 2 pin 26
A0:5	RDAT5	A6	Data5 Probe#2 probe head 2	Mictor 2 pin 28
A0:4	RDAT4	A4	Data4 Probe#2 probe head 2	Mictor 2 pin 30
A0:3	RDAT3	B3	Data3 Probe#2 probe head 2	Mictor 2 pin 32
A0:2	RDAT2	B1	Data2 Probe#2 probe head 2	Mictor 2 pin 34

Table 3-71: Pin connections for SPI3_RX support package (Cont.)

Logic analyzer channel	SPI-3 signal name	P6860 pad name	P6860 probe signal name	AMP Mictor
A0:1	RDAT1	A3	Data1 Probe#2 probe head 2	Mictor 2 pin 36
A0:0	RDAT0	A1	Data0 Probe#2 probe head 2	Mictor 2 pin 38

* **To be connected to ground in case of P6860 probe**

NOTE*. The logic analyzer module end of the P6434 probe cable has two parts (Pin 1 side and Pin 38 side). Connect the Pin 1 side of the module end to D1 and D0 sections of the logic analyzer module. Connect the Pin 38 side of the module end to A1 and A0 sections of the logic analyzer module.*

Refer to the P6434 Mass Termination Probe instruction manual, Tektronix part number 070-9793-03 to identify the Pin 1 side and the Pin 38 side of the AMP Mictor connector.

For example, the P6434 A probe's module end has two sections — Pin 1 side (A3-A2) and Pin 38 side (A1-A0). You should connect the A3-A2 side of the P6434 module end to D1-D0 of the logic analyzer module and A1-A0 side of the P6434 module end to A1-A0 of the logic analyzer module.

Connections for SPI4 and SPI4_LVTTL Supports

The SPI-4.2 supports are common to both the SPI-4.2 Transmit and Receive buses. Therefore:

- TDAT and RDAT are referred to as DAT
- TCTL and RCTL are referred to as CTL
- TSCLK and RSCLK are referred to as SCLK
- TDCLK and RDCLK are referred to as DCLK

When you use the SPI4 and SPI4_LVTTL supports, do not connect the following logic analyzer channels to any signals because they are demuxed.

Qual:0
D3:7-0
D1:7-0
C1:7
C1:6

Figure 3-2 shows a sample of P6880 differential probe land footprint.

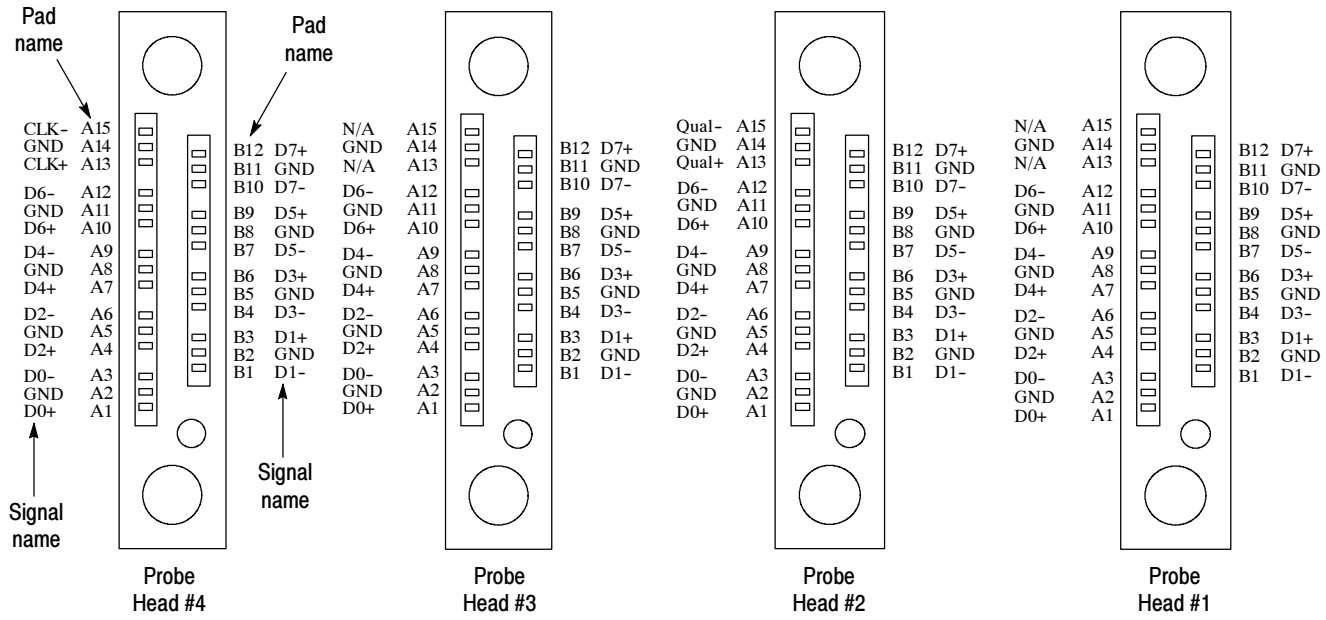


Figure 3-2: Sample of P6880 Differential probe land footprint

Tables 3-72 through 3-76 show the pin connections for the SPI4 and SPI4_LVTTL support packages.

***NOTE**. The flow through the P6880 probe footprint has alternating polarities from channels. That is, the polarity changes between each signal pair: +/-, -/+, +/-, -/+ ensuring correct routing.*

The channel assignments are common for both Transmit and Receive interfaces.

Table 3-72: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#3)

Logic analyzer channel	P6880 probe signal name	P6880 probe #3 probe head 4	P6880 pad name	SPI-4.2 signal name
Clock:0	Clock:0-	CK:0-	A15	DCLK-
	Clock:0+	CK:0+	A13	DCLK+
A3:7	Data7+	A3:7+	B12	DAT7+
	Data7-	A3:7-	B10	DAT7-
A3:6	Data6-	A3:6-	A12	DAT6-

Table 3-72: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#3) (Cont.)

Logic analyzer channel	P6880 probe signal name	P6880 probe #3 probe head 4	P6880 pad name	SPI-4.2 signal name
	Data6+	A3:6+	A10	DAT6+
A3:5	Data5+	A3:5+	B9	DAT5+
	Data5-	A3:5-	B7	DAT5-
A3:4	Data4-	A3:4-	A9	DAT4-
	Data4+	A3:4+	A7	DAT4+
A3:3	Data3+	A3:3+	B6	DAT3+
	Data3-	A3:3-	B4	DAT3-
A3:2	Data2-	A3:2-	A6	DAT2-
	Data2+	A3:2+	A4	DAT2+
A3:1	Data1+	A3:1+	B3	DAT1+
	Data1-	A3:1-	B1	DAT1-
A3:0	Data0-	A3:0-	A3	DAT0-
	Data0+	A3:0+	A1	DAT0+

Table 3-73: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#2)

Logic analyzer channel	P6880 probe signal name	P6880 probe #2 probe head 4	P6880 pad name	SPI-4.2 signal name
Clock:1	Clock:1-	CK:1-	A15	CTL-
	Clock:1+	CK:1+	A13	CTL+
A1:7	Data7+	A1:7+	B12	DAT15+
	Data7-	A1:7-	B10	DAT15-
A1:6	Data6-	A1:6-	A12	DAT14-
	Data6+	A1:6+	A10	DAT14+
A1:5	Data5+	A1:5+	B9	DAT13+
	Data5-	A1:5-	B7	DAT13-
A1:4	Data4-	A1:4-	A9	DAT12-
	Data4+	A1:4+	A7	DAT12+
A1:3	Data3+	A1:3+	B6	DAT11+
	Data3-	A1:3-	B4	DAT11-
A1:2	Data2-	A1:2-	A6	DAT10-
	Data2+	A1:2+	A4	DAT10+
A1:1	Data1+	A1:1+	B3	DAT9+
	Data1-	A1:1-	B1	DAT9-

Table 3-73: Pin connections for SPI4 and SPI4_LVTTL support packages (Probe#2) (Cont.)

Logic analyzer channel	P6880 probe signal name	P6880 probe #2 probe head 4	P6880 pad name	SPI-4.2 signal name
A1:0	Data0-	A1:0-	A3	DAT8-
	Data0+	A1:0+	A1	DAT8+

If SCLK, STAT[1:0] are LVDS signals, use the channel assignments shown in Table 3–74 for the P6880 probe.

***NOTE**. For LVDS signals, the FIFO status clock (SCLK) is the same as DCLK.*

Table 3-74: Pin connections for SPI4 support package for FIFO Status LVDS signals (Probe#1)

Logic analyzer channel	P6880 probe signal name	P6880 probe #1 probe head 4	P6880 pad name	SPI-4.2 signal name
C3:7	Data7+	C3:7+	B12	STAT1+
	Data7-	C3:7-	B10	STAT1-
C3:6	Data6-	C3:6-	A12	STAT0-
	Data6+	C3:6+	A10	STAT0+

If SCLK, STAT[1:0] are LVTTL signals, use the channel assignments shown in Table 3–75 for the P6880 probe.

Table 3-75: Pin connections for SPI4_LVTTL support package for FIFO Status LVTTL signals (P6880)

Logic analyzer channel	P6880 probe signal name	P6880 probe #1 probe head 4	P6880 pad name	SPI-4.2 signal name
Clock:3	Clock:3-	CK3-	A15	GND
	Clock:3+	CK3+	A13	SCLK
C3:7	Data7+	C3:7+	B12	STAT1
	Data7-	C3:7-	B10	GND
C3:6	Data6-	C3:6-	A12	GND
	Data6+	C3:6+	A10	STAT0

If SCLK, STAT[1:0] are LVTTL signals, use the channel assignments shown in Table 3–76 for the P6860 probe.

Table 3-76: Pin connections for SPI4_LVTTL support package for FIFO Status LVTTL signals (P6860)

Logic analyzer channel	P6860 probe signal name	P6860 probe #1 probe head 2	P6860 pad name	SPI-4.2 support signal name
Clock:3	Clock:3-	CK3-	A15	GND
	Clock:3+	CK3+	A13	SCLK
C3:7	Data15	C3:7	B12	STAT1
C3:6	Data14	C3:6	B10	STAT0

Signal Acquisition

This section contains timing diagrams that explain how the TCS101 product acquires the relevant address, data, and control signals for the SPI3_TX, SPI3_RX, SPI4, and SPI4_LVTTL support packages.

Signal Acquisition in SPI-3

Figure 3–3 shows the timing diagram for the SPI-3 32-bit transmit bus when the clocking option “Active Cycles” is selected.

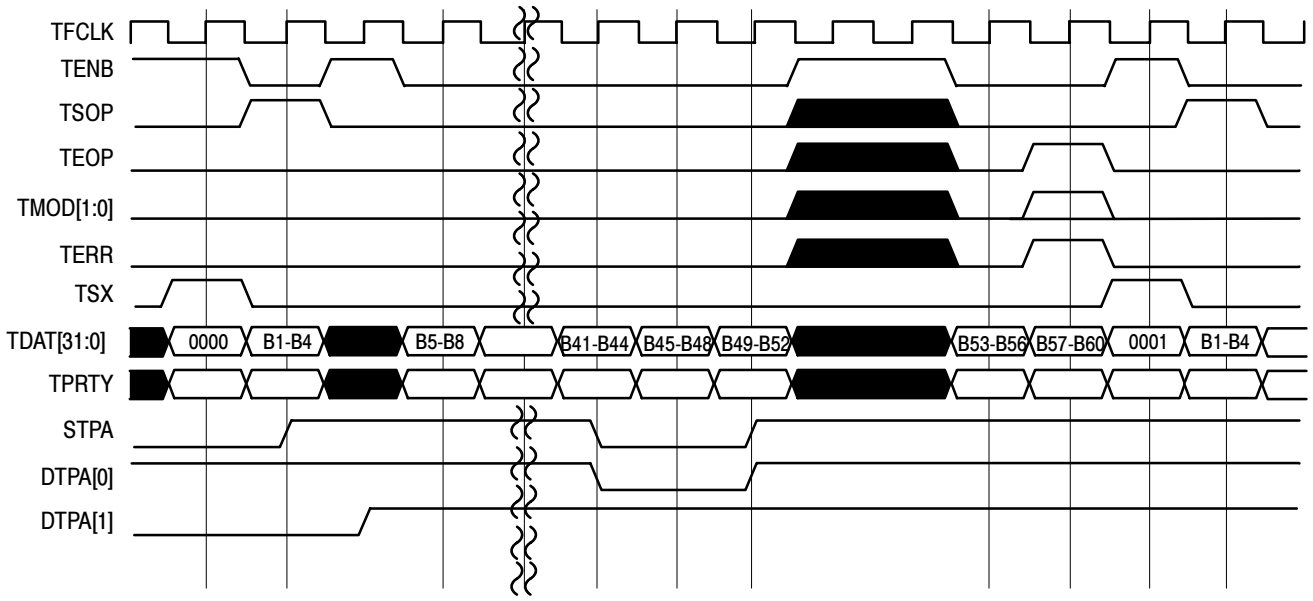


Figure 3–3: Example of a timing diagram for the transmit bus with clocking option “Active Cycles” selected

The data points that are sampled by the SPI3_TX support at the rising edge of the clock are indicated by vertical lines. In general, the support package samples the bus only when the TENB is low. However, if TENB is high and TSX is high, the support package samples the in-band address from the TDAT lines. You must choose the proper clocking option to acquire the in-band address.

When you select the clocking option “All”, the SPI3_TX support acquires data at each rising edge of the clock.

Figure 3–4 shows the timing diagram for the SPI-3 8-bit receive bus when the clocking option “Active Cycles” is selected.

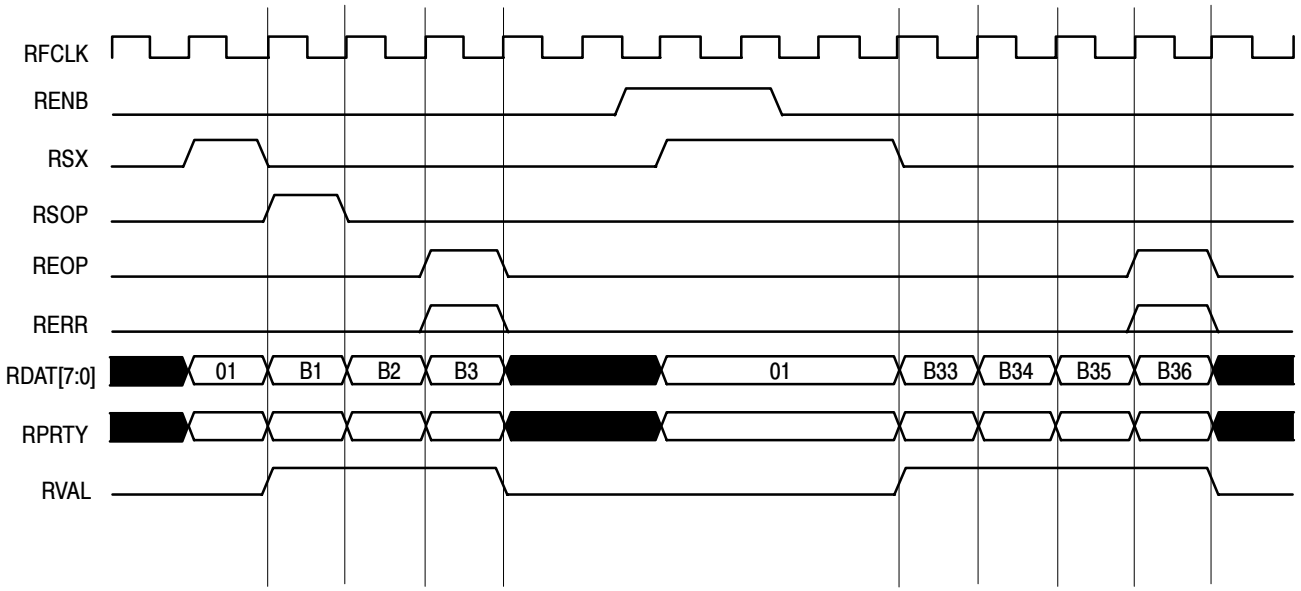


Figure 3–4: Example of a timing diagram for the receive bus with clocking option “Active Cycles” selected

The data points that are sampled by the SPI3_RX at the rising edge of the clock are indicated by vertical lines. In general, the support package samples the bus only when RVAL is high and RENB was low in the previous sample. However, if RSX is high, RVAL is low, and RENB was low in the previous sample, the support package samples the in-band address from the RDAT lines. You must choose the proper clocking option to acquire the in-band address.

When you select the clocking option “All”, the SPI3_RX support acquires data at each rising edge of the clock.

Signal Acquisition in SPI-4.2

The SPI4 and SPI4_LVTTL setup software acquires the rising and falling edge data together in a single 32-bit sample. The raw data is available by viewing the DATA channel group. The DAT[31:16] channels correspond to the falling edge data and DAT[15:0] channels correspond to the rising edge data. Similarly, the CTL group has two channels — CTL_DM and CTL. CTL_DM is for DAT[31:16] and CTL is for DAT[15:0].

The SPI4 support package also acquires LVDS FIFO Status signals. The SPI4_LVTTL support package also acquires LVTTL FIFO Status signals.

Figure 3–5 shows a timing diagram for the SPI-4.2 bus.

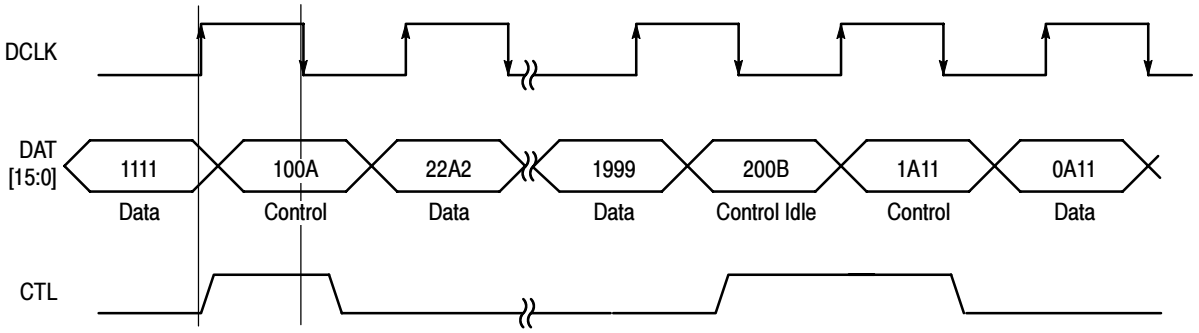


Figure 3–5: Example of a timing diagram for the SPI-4.2 bus

Specifications

Specifications

This section contains the specifications for the TCS101 product.

Specification Table

Table 4–1 lists the electrical requirements that the target system must produce for the support to acquire correct data.

Table 4–1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
TCS101 specified clock rate for SPI3_TX and SPI3_RX support packages	The maximum rates are 120, 200, 235, 450 MHz depending upon the type of logic analyzer module
TCS101 specified clock rate for SPI4 and SPI4_LVTTL support packages	Maximum 350 MHz[1]
Minimum setup time required for the	
Logic analyzer TLA7Axx	0.750 ns
Minimum hold time required for the	
Logic analyzer TLA7Axx	0 ns
Minimum setup time required for the	
Logic analyzers TLA7xx, TLA6xx	2.5 ns
Minimum hold time required for the	
Logic analyzer TLA7xx, TLA6xx	0 ns

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest bus supported.**

Index

Index

A

B

C

D

E

F

H

I

L

M

N

O

P

Q

R

S

T

U

V

W